SAMPLE STUDY MATERIAL

Electronics Engineering

EC/E & T

Postal Correspondence Course

GATE , IES & PSUs

Microprocessor

CONTENT

CHAPTER - 1

MICROPROCESSOR 8085

- A microprocessor unit is generally referred as MPU
- MPU is designed with ALU, control unit and some count of processing Registers and these registers are used to store the data temporarily during program execution
- Generally different MPUs available are specified like 8 bit, 16 bit, 32 bit and so on.
- Bit capacity of MPU is defined as the no.of bits it can process at a time in parallel .i.e. an 8 bit MPU can perform all 8 bit operations at a time
- In general, the internal architecture of the microprocessor depends on the bit capacity of the micro processor
- The system bus of MPU consist of 3 types of buses known as address bus ; data bus and control bus.
- Address signals are generated by MPU and sent to memory to identify the address of the memory through address bus and it is unidirectional bus.
- Data bus is used to transfer the data in between memory and MPU
- Control signals are generated by MPU and these signals are transferred in between memory and MPU and used to provide timing for various operations
- Control signals are used to perform the required operations.
- MPU can primarily perform 4 operations ; Memory Read ; Memory write ; I/O Read and I/O write; and for each operation it generates the appropriate control signals

8085 Microprocessor

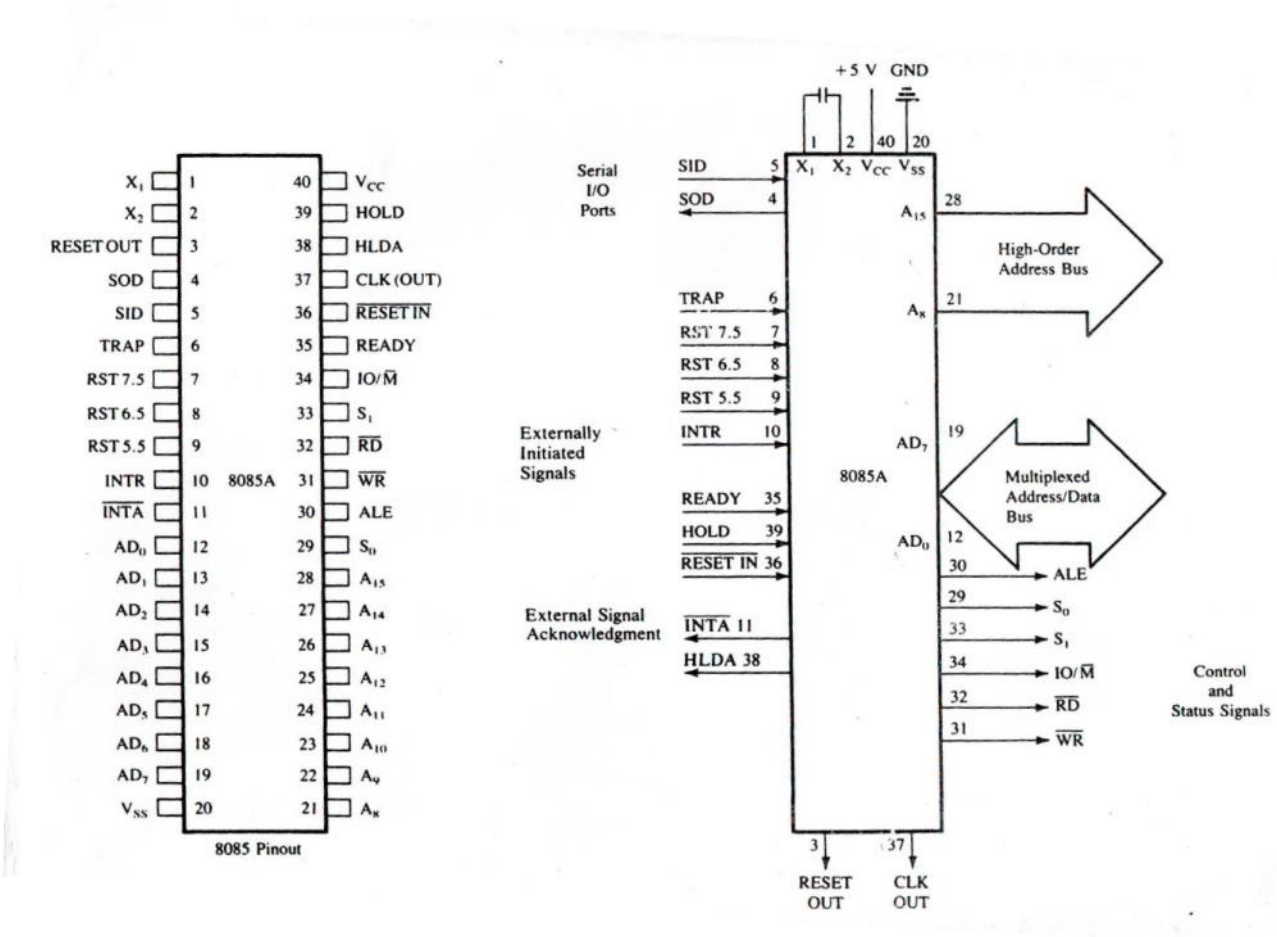
- It is a 40 pin I.C with operating voltage 5 volts
- It is designed with 2 MH and 3.07 MHz frequencies
- Max clock frequency of 8085 is 3.07 MHz (3MHZ)
- Crystal frequency is double to its clock
- 8085 MPU is designed with on chip clock generator i.e. no external oscillator is required

- 8085 MPU has 74 basic instructions and 246 opcodes
- 8085 supports 5 no.of hardware interrupts and 8 no.of software interrupts

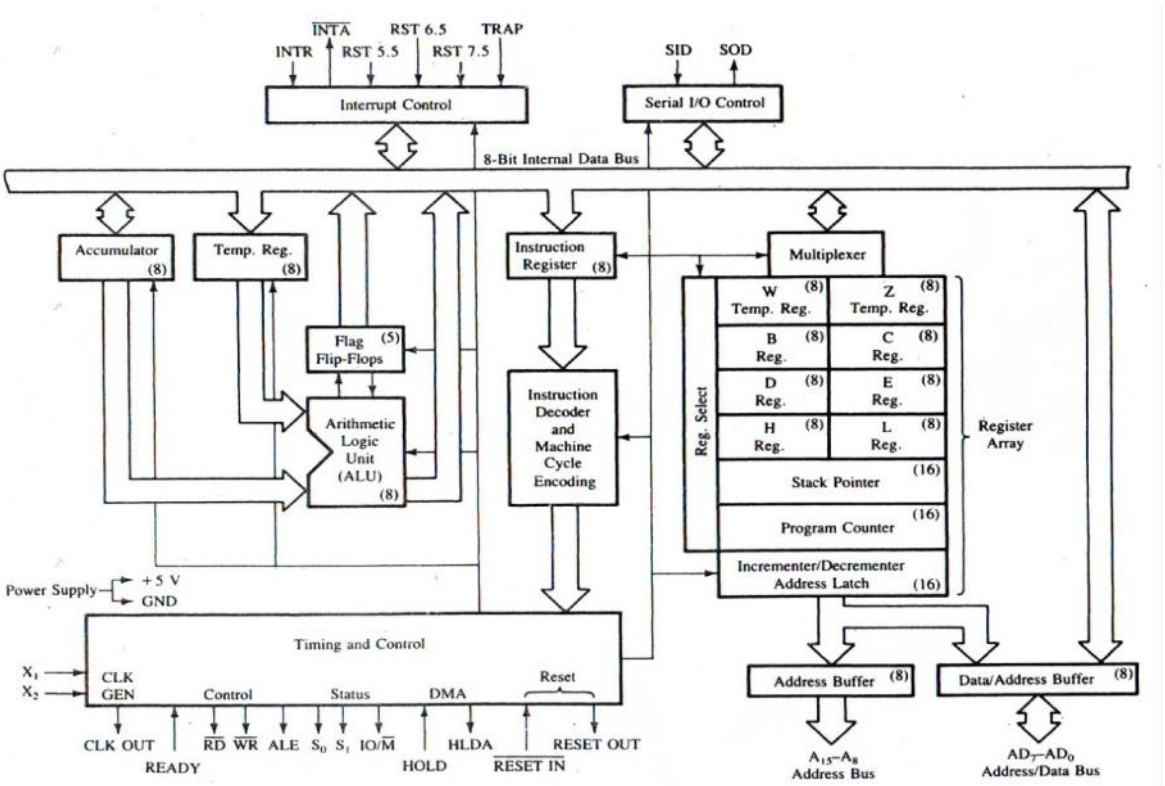
- Hardware interrupts are Trap ; RST 7.5; RST 6.5; RST 5.5 and INTR
- Trap has the highest priority among all
- But trap has lower priority than DMAC during DMA
- Trap is also known as RST 4.5
- INTR has the lowest priority
- No.of software interrupts for 8085 are 8, and range from RST '0' to RST '7'
- Opcode length varies from 1 byte to 3 byte
- Instructions, having the 16 bit address in the given instruction known as 3 byte instructions Ex : Call 2500H
- Instructions, having the 8 bit data or port address in the given instruction is 2 byte instruction Ex : MVI A, 35H
- Instruction with neither 16 bit address nor 8 bit data is known as 1 byte instruction Ex : MOV A, B
- In 8085 MPU ; 5 No.of flags are available and these flags are also known as status flags; known as carry (cy) ; Auxilary carry (Ac) ; Sign (s) ; parity (P) and zero (z)
- 8085 MPU has 2 no.of 16 bits Registers known as program counter (PC) and stack pointer (SP)
- PC always holds the address of the next instruction to be executed
- SP always holds the address of the top of the stack
- 8085 MPU has 8 bit accumulator and 8 bit flag Register ; and this combination is known as PSW (Program status word)
- 8085 MPU is designed with 6 no.of general purpose registers along with A and F ; these register are known as B, C ; D E and H, L.
- These 8 bit general purpose register can be used as 3 no.of 16 bit Register Pairs when required like BC, DE and HL pairs
- 8085 MPU has 16 no.of address lines and 8 no.of data lines
- Memory size of any MPU depends on the no.of address lines
- Total no.of Memory locations that can be accessed by 8085 MPU is 2^{16} =64 K = 65536
- In Hex code ; the memory ranges from 0000 H to FFFFH
- The lower 8 no.of address lines are multiplexed with 8 data lines and specified as AD_0 to AD_7
- Multiplexing of address and data lines is used to reduce the hardware size of MPU
- The no.of Machine clycles required to execute an 8085 MPU instruction varies from one of five

- Max no.of 'T' states for executing an instruction are 18 and minimum no.of 'T' states required for executing an instruction are 4
- Max no.of machine cycles required are 5 and minimum one
- 'T' state value depends on the clock frequency
- Group of 'T' states is known as machine cycle
- Group of machine cycles is known as execution cycle

Signal description of 8085 MPU



The 8085A Microprocessor Functional Diagram



- Total no.of signal pins (40) are divided in to 6 Groups
  1) Power supply and frequency
  2) serial I/O ports
  3) Address Bus
  4) Data bus
  5) Interrupts and externally initiated signals
  6) Status, control and Acknowledge signals
- SID and SOD signals are used for serial communication
- SIM and RIM instructions are used for serial I/O communication
- A.L.E. is used to generate the lower order address lines (A, → A_0)
- S_1, S_0 and IO/$\overline{M}$ signals are called status signals
- $\overline{RD}$ and $\overline{WR}$ signals are control signals

- HOLD and HLDA are used for DMA operation
- READY signal is used by the MPU to communicate with slow operating peripherals
- $\overline{RESETIN}$ is active low signal to chip Reset
- RESET out signal is used to connect to RESETIN of other inter facing circuits used in microprocessor based system
- CLOCKOUT of 8085 will be connected to CLOCKIN of other interfacing ckts used in microprocessor based system to synchronize the operation with 8085
- So and S_1 signals are used to indicate the current status of the processor

S_1	S_0	Status
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

- The process of getting / reading the opcode from memory to C.P.U is known as opcode fetch
- The process of getting / reading the data from memory is known as operand fetch
- By combining the status signals IO/ $\overline{M}$ with control signals $\overline{RD}$ and $\overline{WR}$ we can generate the following operations, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$

IO/ $\overline{M}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	1	Memory Read
0	1	0	Memory write
1	0	1	I/O Read
1	1	0	I/O Write

- All software interrupts are vectored interrupts
- Hardware interrupts are of 2 types a) vectored interrupts b) Non – vectored interrupts
- RST 7.5, RST 6.5, RST 5.5, and RST 4.5 are called Hardware vectored interrupts
- INTR is called Hardware non vectored interrupt
- Interrupts vectored address

TRAP	0024H
RST 5.5	002CH
RST 6.5	0034H
RST 7.5	003CH
RST 0	0000H
RST 1	0008H
RST 2	0010H
RST 3	0018H
RST 4	0020H
RST 5	0028H
RST 6	0030H
RST 7	0038H

- TRAP is a nonmaskable interrupt and always in enable condition
- RST 7.5, 6.5, 5.5 and INTR are maskable and these interrupts can be enabled / disabled by EI and DI instructions respectively
- RST 7.5, RST 6.5, and RST 5.5 interrupts can be masked or unmasked by using SIM instruction
- RST 7.5 is edge triggered interrupt
- RST 6.5, RST 5.5 and INTR are level triggered interrupts
- TRAP is both level triggered and edge triggered interrupt
- SIM instruction is used for serial out put data operation as well as to mask or unmask different maskable interrupts
- RIM instructions is used for serial input data operations as well as to read the status of different maskable interrupts
- 8085 MPU has an 8 bit flag Register
- In flag Register ; Out of 8 bits, 5 bits are used to represent valid flags and remaining 3 bits are don't cares
- These flags are set / Reset according to the data conditions in the accumulator and other Registers
- Flags are affected by the arithmetic and logical operations in the ALU.
- Flags are used to reflect the data conditions in the ALU
- Position of different flags in flag Register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	CY

- MSB in the flag Register is used to indicate the sign of the result for signed data during Arithmetical operations and remaining 7 bits are used to represent the magnitude of the number
- After execution, if sign flag is set ; it indicate the result is Negative, the result is positive when it is reset
- If zero flag is set, then ALU operation result is zero
- Auxilary carry flag is used during BCD addition
- AC flag is set when there is a carry from lower nibble to higher nibble
- Parity flag will be set, when the result has an even no.of ones
- Carry flag is also considered as Borrow flag during subtraction operation
- During addition the carry flag is '1' when the result has 9 bits during 8 bit addition
- Borrow flag is '1' when the subtraction operation is performed in between lower value and Higher value

Instruction set :

- Instruction set of 8085 MPU can be classified on their operation as the following Groups
  a) Data transfer b) Arithmetical
  c) Logical d) Branch
  e) Machine control

Data transfer instructions :

- These are used to transfer the data in between Register to Register or from Register to Memory
- No flags will be affected
- Different – Mnemonics are

  MOV, MVI, LXI, LDA, STA, LHLD,

  SHLD, LDAX, STAX, XCHG, AND PCHL

Arithmetical instructions :

- In 8085 : the possible operations are Addition subtraction, increment and decrement
- 8085 MPU does not support multiplication and divisions operations
- AC flag is used during the execution of DAA

- For INX and DCX instructions ; no flags will be affected
- For INR and DCR, carry flag is not affected
- For DAD operation only carry flags may be affected
- Different Arithmetic mnemonics are ADD, ADI, ADC, SUB, SUI, SBB, SBI, INR, INX, DCR, DCX, DAD and DAA

Logical instructions :

- During execution ; flags may be modified
- Carry flag = 0 during AND, OR, XOR execution
- Only carry flag may be modified during the execution of RLC, RRC, RAL, STC, CMC,
- Different mnemonics are ORA, ORI, ANA, ANI, XRA, XRI, CMP, CPI, CMA, CMC, STC, RLC, RAL, RRC, RAR

Branch Instructions :

- These are also called as program control instructions
- These are divided into conditional unconditional
- No flags will be affected
- For executing the conditional Branch instructions it is compulsory to check the condition of respective flag, assigned in the instruction
- All jump and CALL instructions have 16 bit address
- No address is required for RET instruction
- PCHL is one byte and equivalent of 3 byte Jump instruction
- RST 'n' is one byte and equivalent of 3 byte call instruction
- Un conditional Branch instructions :

  JMP, CALL, RET, RSTn, (n = 0 to 7) and PCHL
- Conditional Branch Instructions :

  JZ, JNZ, JC, JNC, JP, JM, JPO, JPE, CZ, CNZ, JC, CMC, CP, CM,

  CPO, CPE, RZ, RNZ, RC, RNC, RP, RM, RPO and RPE

Machine control Instructions.

- EI, DI, SIM, RIM, NOP, HLT, OUT and IN; PUSH PSW; POP PSW; LXI SP, SPHL, XTHL, and STC
- IN and OUT instructions have 8 bit port address
- When PUSH instruction is executed, SP Register content is decremented by 2
- When POP instruction is executed SP Register content is incremented by 2
- When CALL instruction or RST instruction is executed, SP Register content is decremented by 2, because current content of PC will be pushed automatically on the top two locations of the stack.
- When RET instruction is executed, SP register content is incremented by 2, because microprocessor retrieves address from top two locations of the stack and loaded in to P.C
- Comparison of PUSH and POP instructions with CALL and RET instructions

PUSH and POP	CALL and RET
The programmer uses the instruction PUSH to save the contents of specified Register pair on the stack	When CALL is executed ; the micro processor automatically stores the 16 bit address of the next instruction to CALL on the Stack
When push is executed ; the SP is decremented by 2	When CALL is executed, the SP is decremented by 2
The instruction POP transfer the contents of top two locations of the stack to the specified Register Pair	The instruction RET transfers the content of the top 2 locations of the stack to program counter
When the instruction POP is executed, the SP is incremented by 2	When the instruction RET is executed, the SP is increment by 2
There are no conditional PUSH and POP instructions	There unconditional CALL and RET instructions along with conditional instructions

ADDRESSING MODES

>> It is the process of way of locating the operand (data)

- 8085 MPU supports 5 addressing modes

Implied Addressing mode : It is also known as implicit or Absolute addressing mode

- This addressing mode is used to perform the given operation on the content of Accumulator Ex : CMA, STC, RRC, RLC, RAR, etc.

Register Addressing mode : In this ; the operands are in the general purpose Register

- The opcode specifies the address of the Register in addition to the operation to be performed Ex : MOV A, B ; ADD B ; SUB C

Immediate Addressing mode : In this mode ; the operand is specified in the instruction it self Ex : MVI, ADI, ORI, LXI, SBI, SUI, ANI, XRI

Direct Addressing mode : In this ; the address of the operand is given in the given instruction Ex : STA, LDA, SHLD, LHLD, IN, OUT etc

Indirect addressing mode : In this addressing mode ; the address of the operand is specified by a Register Pair. Ex : STAX, LDAX, ADDM, DCRM.

In indirect addressing mode ; HL pair is used as memory pointer